**How to Use FIFO**

**Location of Files:**

The location of the fifo.v module and testbench is GitHub\Chip-Design\proj\_asic\rtl\FIFO.

**Macros:**

* BUF\_WIDTH: number of bits used for the addressing of the fifo
* BUF\_SIZE: number of elements allowed in the buffer =
* DATA\_SIZE: no of bits of the input and output data

**Inputs:**

* clk: master clock
* rst: reset
* fifo\_inp\_data [DATA\_SIZE-1:0]): input data
* fifo\_inp\_rts: write client asserts Ready-To-Send
* fifo\_out\_rtr: read client asserts Ready-To-Receive

**Outputs:**

* fifo\_out\_data [DATA\_SIZE-1:0]: output data
* fifo\_out\_rts: output fifo asserts Ready-To-Send
* fifo\_inp\_rtr: output fifo asserts Ready-To-Receive

**Example:**

If the FIFO needed to hold 8 elements we would specify the BUF\_WIDTH to be 3. If we wanted the input and output data to be 16 bits we would specify the DATA\_SIZE to be 16. This is done in the FIFO module by writing:

`define BUF\_WIDTH 3

`define BUF\_SIZE ( 1<<`BUF\_WIDTH )

`define DATA\_SIZE 16